Sub A1

CLAIMS

1. A method comprising:

receiving a plurality of commands to access at least one of a plurality of memory banks of a memory; and

scheduling the plurality of commands based at least in part on a status information of at least one of the plurality of memory banks.

2. The method of claim 1 wherein the memory is a synchronous dynamic random access memory.

3. The method of claim 1 wherein the status information based at least in part on an idle state of the plurality of memory banks with respect to a bank based queuing scheme.

4. The method of claim 1 wherein the status information is either an idle state of the plurality of memory banks.

5. The method of claim 1 wherein the status information is based at least in part on a type of a most recent command forwarded to the memory device via a memory bus.

6. The method of claim 1 wherein the plurality of commands are read and write commands.

7. A system comprising:

a processor; and

a logic, coupled to the processor and to at least one memory device with a plurality of memory banks, to receive commands to access the memory device and to schedule the commands based at least in part on a status information of the plurality of memory banks..

8. The system of claim 7 wherein the commands are read and write commands.

9. The system of claim 7 wherein the wherein the status information is based at least in part on a type of most recent command forwarded to the memory device via a memory bus.

10. The system of claim 7 wherein the plurality of memory banks perform in parallel.

11. The system of claim 7 wherein the logic is a network switch or a memory controller.

12. The system of claim 7 wherein the status information is an idle state of the plurality of memory banks.

13. The system of claim 7 wherein the memory is a synchronous dynamic random access memory.

14. An apparatus comprising:

a first logic, coupled to at least one memory device with a plurality of memory banks, to receive commands to access the memory device; and

a second logic, coupled to the first logic, to schedule the received commands based at least in part on a status information of the plurality of memory banks.

15. The apparatus of claim 14 further comprising a third logic to forward the schedule of the received commands to the memory device via a memory bus.

16. The apparatus of claim 14 wherein the apparatus is either one of a network switch or memory controller.

17. The apparatus of claim 14 wherein the memory device is a synchronous dynamic random access memory.

18. The apparatus of claim 14 wherein the received commands are read and write commands.

19. The apparatus of claim 14 wherein the status information is based at least in part on a type of most recent command forwarded to the memory device via the memory bus.

20. The apparatus of claim 14 wherein the plurality of memory banks perform in parallel.

21. The apparatus of claim 14 wherein the status information is an idle state of the plurality of memory banks.

22. A method comprising:

receiving a plurality of commands to access at least one of a plurality of memory banks of a memory coupled to a memory bus;

scheduling the plurality of commands based at least in part on a status information of at least one of the plurality of memory banks; and

arbitrating between the commands to determine priority of access to the memory bus.

23. The method of claim 22 wherein the memory is a synchronous dynamic random access memory.

24. The method of claim 22 wherein the status information is an idle state of the plurality of memory banks.

25. The method of claim 22 wherein the plurality of memory banks perform in parallel.

26. The method of claim 22 wherein the status information is based at least in part on a type of a most recent command forwarded to the memory device via a memory bus.

27. The method of claim 22 wherein the plurality of commands are read and write commands.

28. An article comprising:

a storage medium having stored thereon instructions, that, when executed by a computing platform, result in forwarding a plurality of commands to a memory device by:

receiving the plurality of commands to access at least one of a plurality of memory banks of the memory device; and

scheduling the plurality of commands based at least in part on a status information of at least one of the plurality of memory banks.

29. The article of claim 28 wherein the memory is a synchronous dynamic random access memory.

30. The article of claim 28 wherein the status information is an idle state of the plurality of memory banks.

31. The article of claim 28 wherein the plurality of memory banks perform in parallel.

32. The article of claim 28 wherein the status information is based at least in part on a type of a most recent command forwarded to the memory device via a memory bus.

33. The article of claim 28 wherein the plurality of commands are read and write commands.